AMENDMENT TO THE SPECIFICATION

Please amend the paragraph beginning at page 6, line 4, as follows:

A chip select signal Cs_L, a row address strobe signal Ras_L, a column address strobe signal Cas_L, a write enable signal We_L, an address signal addr and the clock enable signal ClkE are outputted from the memory controller 11 to the SDRAM 12 to control the SDRAM 12. Incidentally, the signals denoted by "_L" are low active signals which become active (effective) at a low level. The signal ClkE is a high active signal. Further, a ~~date~~ data signal ~~Date~~ Data is communicated between the memory controller 11 and the SDRAM 12.

Please amend the paragraph beginning at page 7, line 2, as follows:

When the main power supply Vcc is turned ON, the system reset signal Reset_L is changed to the low level. When the signal Reset_L is in the low level, since the signal RamBackUp is also in the low level, the memory controller 11 holds the signals Cs_L, Ras_L, Cas_L, We_L and ClkE to high levels. ~~when~~ When the signal Reset_L is cancelled, since the signal RamBackUp is changed to the low level, power-on initial sequence of the SDRAM 12 is effected (~~Pre-Change~~ Pre-Charge All command is issued, and thereafter, Auto Refresh Commands are issued by 8 times and Mode Set Command is issued), and, thereafter, normal operation is performed, and, if necessary, read/write of the SDRAM 12 is effected.